

IN THE CLAIMS:

Please amend the claims, as follows:

Claim 1. (currently amended): A method for the selection (puncturing) of data bits from a data word in a data processing system, notably a communication system, comprising the steps of:

providing a selection bit register which contains n selection bits associated with said data bits of said data word;

~~wherein the~~ selecting data bit or data bits of the data word comprising n data bits ~~are selected,~~ within one cycle of operation of a working processor, on the basis of ~~[[a]]~~ the selection bit register which contains, wherein each of the n selection bits which ~~indicate~~ indicates whether a corresponding data bit of the data word is to be selected; and

writing said selected data bits into a buffer memory and summing the number of data bits written in the buffer memory.

Claim 2. (canceled)

Claim 3. (previously presented): A method as claimed in claim 1, wherein the data bits selected within one cycle of operation are counted.

Claim 4. (canceled)

Claim 5. (currently amended): A method as claimed in claim 2, wherein prior to the writing of a number of new data bits, the data bits that are already present in the

buffer memory which is constructed as a shift register are shifted ~~through~~ over the number of new data bits ~~prior to the writing of new data bits.~~

Claim 6. (currently amended): A method as claimed in claim 1, wherein the selected data bits, possibly already present in the buffer memory, are prepared so as to form an output data word, while utilizing a working bit register which contains m working bits and defines the output format, for output to a memory ~~or the like.~~

Claim 7. (original): A method as claimed in claim 6, wherein the output takes place in dependence on the number of data bits present in the buffer memory or after every cycle of operation of the working processor.

Claim 8. (previously presented): A method as claimed in claim 6, wherein a predetermined number of data bits is output from the buffer memory.

Claim 9. (previously presented): A method as claimed in claim 6, wherein the data word read out from the buffer memory is extended by the addition of one or more further data bits.

Claim 10. (previously presented): A method as claimed in claim 6, wherein the data word read out from the buffer memory is shifted within the output data word.

Claim 11. (previously presented): A device for carrying out the method claimed in claim 1, including a working processor (2) and a data bit selection unit (1) for selecting

one or more given data bits from a data word (4), comprising n data bits (10), on the basis of a selection bit register (6) which contains n selection bits (11) which indicate whether a data bit (10) of the data word (6) is to be selected, such selection taking place within one cycle of operation of the working processor (2).

Claim 12. (original): A device as claimed in claim 11, characterized in that the selection bit register (6) can be loaded from a selection bit register memory (5) which comprises a plurality of selection bit registers (6) and is included in the data bit selection unit (1).

Claim 13. (previously presented): A device as claimed in claim 11, characterized in that there is provided a buffer memory (7) which is constructed as a shift register and in which the data bits (10) selected within one cycle of operation can be stored.

Claim 14. (previously presented): A device as claimed in claim 11, characterized in that there is provided a counter for counting the data bits (10) selected within one cycle of operation and for summing the numbers of bits of a plurality of cycle of operation.

Claim 15. (previously presented): A device as claimed in claim 13, characterized in that data bits already present in the buffer memory (7) can be shifted in dependence on the number of new data bits (10) to be written.

Claim 16. (previously presented): A device as claimed in claim 11, characterized

in that there is provided at least one working bit register (8) which contains m working bits (14) and defines the output format, said working bit register preparing data bits read out from the buffer memory (7) so as to be output in the form of an output data word (9).

Claim 17. (currently amended): A device as claimed in claim 16, characterized in that the working bit register (8) includes a first register section (I) which constitutes ~~[[the]]~~ a counter.

Claim 18. (previously presented): A device as claimed in claim 16, characterized in that there is provided a second counter section (II) which defines the number of data bits (13) to be read out from the buffer memory (7).

Claim 19. (previously presented): A device as claimed in claim 16, characterized in that there is provided a third register section (III) whereby the data bits (15) read out can be shifted within the output data word (9).

Claim 20. (currently amended): A device as claimed in claim 16, characterized in that there are provided a fourth and a fifth register section (IV, V) which define how the output data word (9), consisting of m data bits (15), is to be completed when n data bits are read out from the buffer memory (7), where $n < m$.

Claim 21. (previously presented): A device as claimed in claim 16, characterized in that there is provided a sixth register section (VI) whereby the output mode can be

adjusted.

Claim 22. (currently amended): A device as claimed in claim 21, characterized in that a first bit is written or can be written into the sixth register section (VI) and a selection between a first output mode in which the updating of a pointer, that can be updated before or after reading out and indicates a memory location, is suppressed until the count of the counter is smaller than or equal to ~~[[the]]~~ a defined number, and a second mode in which updating of the pointer is permitted, irrespective of the count, is made on the basis of the value of the bit written in the sixth register section (VI).

Claim 23. (previously presented): A device as claimed in claim 11, characterized in that it forms part of a portable telecommunication device for mobile telecommunication.

Claim 24. (new): A method for the selection (puncturing) of data bits from a data word in a data processing system, notably a communication system, comprising the steps of:

providing a selection bit register which contains n selection bits associated with said data bits of said data word; and

selecting data bit or data bits of the data word comprising n data bits within one cycle of operation of a working processor, on the basis of the selection bit register, wherein each of the n selection bits indicates whether a corresponding data bit of the data word is to be selected; and

preparing said selected data bits so as to form an output data word, while

utilizing a working bit register which contains m working bits and defines the output format, for output to a memory.

Claim 25. (new): A method for the selection (puncturing) of data bits from a data word in a data processing system, notably a communication system, comprising the steps of:

providing a selection bit register which contains n selection bits associated with said data bits of said data word; and

selecting data bit or data bits of the data word comprising n data bits within one cycle of operation of a working processor, on the basis of the selection bit register , wherein each of the n selection bits indicates whether a corresponding data bit of the data word is to be selected; and

writing said selected data bits into a buffer memory constructed as a shift register so that prior to the writing of a number of new data bits, the data bits that are already present are shifted over the number of new data bits.